CLAIMS

1. A low noise amplifier with a MIS transistor, which amplifies an input signal suppressing the noise to a low level, wherein the MIS transistor comprises:

a semiconductor substrate for comprising a first crystal plane as a principal plane;

a semiconductor structure, formed as a part of the semiconductor substrate, for comprising a pair of sidewall planes defined by the second crystal plane different from the first crystal plane and a top plane defined by the third crystal plane different from the second crystal plane;

a gate insulator for covering the principal plane, the sidewall planes and the top plane of uniform thickness;

a gate electrode for continuously covering the principal plane, the sidewall planes and the top plane on top of the gate insulator; and

a single conductivity type diffusion region formed in one side and other side of the gate electrode in the semiconductor substrate and the semiconductor structure and continuously extending along the principal plane, the sidewall planes and the top plane.

2. A low noise amplifier with a MIS transistor, which amplifies an input signal suppressing the noise to a low level, wherein the MIS transistor comprises:

a semiconductor substrate comprising a projecting part of which the surfaces are at least two different crystal planes on a principal plane;

a gate insulator for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part;

a gate electrode comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on each of said at least two different crystal planes constituting the surface of the projecting part; and

a single conductivity type diffusion region formed in the projecting part facing each of said at least two different crystal planes constituting the surface of the projecting part and individually formed on both sides of the gate electrodes.

3. A low noise amplifier with a MIS transistor, which amplifies an input signal suppressing the noise to a low level, wherein the MIS transistor is a three-dimensional MIS transistor comprising:

a semiconductor substrate comprising at least two

crystal planes;

a gate insulator formed on at least two of the crystal planes on the semiconductor substrate; and

a gate electrode formed on the semiconductor substrate sandwiching the gate insulator,

in which when voltage is applied to the gate electrode, a channel width of a channel formed in the semiconductor substrate along with the gate insulator is represented by summation of each channel width of the channels individually formed on said at least two crystal planes.

4. The low noise amplifier according to any of claim 1 to claim 3, wherein the MIS transistor is characterized in:

that the semiconductor substrate is a silicon substrate; and

that a gate insulator on a surface of the silicon substrate, is formed by removing hydrogen in a way that the surface of the silicon substrate is exposed to plasma of a prescribed inert gas, and the hydrogen content at an interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density.

5. The low noise amplifier according to claim 4,

wherein said at least two crystal planes are any two different crystal planes from a (100) plane, a (110) plane and a (111) plane.

6. A low noise amplifier, comprising a CMOS transistor configured in an n-channel MOS transistor and a p-channel MOS transistor, wherein at least one of the n-channel MOS transistor or the p-channel MOS transistor comprises the MIS transistor of the low noise amplifier according to claim 1 or claim 3.

7. The low noise amplifier according to claim 6 wherein element areas and current driving capacities of the p-channel MOS transistor and the n-channel MOS transistor closely agree with each other.

8. The low noise amplifier according to claim 6 wherein

input voltage based on the input signal is applied to both the gate of the p-channel MOS transistor and the gate of the n-channel MOS transistor,

a voltage source is configured at the drain side of the p-channel MOS transistor,

the source of the p-channel MOS transistor and the drain of the n-channel MOS transistor are mutually

connected,

a direct current feedback circuit for operating point determination is connected between the source and the drain of the n-channel MOS transistor, and

voltage, present in the connection line mutually connecting the source of the p-channel MOS transistor and the drain of the n-channel MOS transistor, being output as the amplified voltage of the input voltage.

9. The low noise amplifier according to claim 7 wherein

input voltage based on the input signal is applied to both the gate of the p-channel MOS transistor and the gate of the n-channel MOS transistor,

a voltage source is configured at the drain side of the p-channel MOS transistor,

the source of the p-channel MOS transistor and the drain of the n-channel MOS transistor are mutually connected,

a direct current feedback circuit for operating point determination is connected between the source and the drain of the n-channel MOS transistor, and

voltage, present in the connection line mutually connecting the source of the p-channel MOS transistor and the drain of the n-channel MOS transistor, being

output as the amplified voltage of the input voltage.

10. The low noise amplifier according to any of claim 1 to claim 3, which is used in a direct conversion receiving system.